



STS26N3LLH6

N-channel 30 V, 0.0038 Ω , 26 A, SO-8
STripFET™ VI DeepGATE™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STS26N3LLH6	30 V	0.0044 Ω	26 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge

Applications

- Switching applications

Description

This product utilizes the 6th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

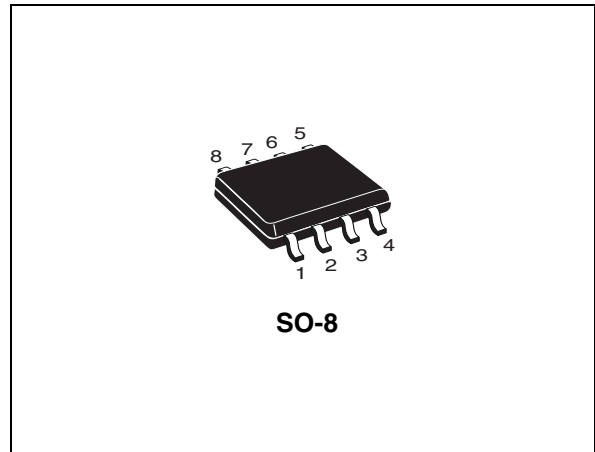


Figure 1. Internal schematic diagram

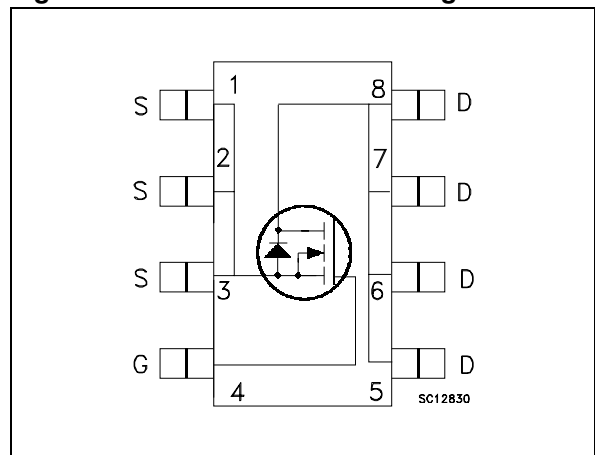


Table 1. Device summary

Order code	Marking	Packag	Packaging
STS26N3LLH6	26G3L	SO-8	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	10
5	Revision history	13

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
$V_{GS}^{(1)}$	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	26	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	16.25	A
$I_{DM}^{(2)}$	Drain current (pulsed)	104	A
P_{TOT}	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.7	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Continuous mode
2. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient	47	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current	40	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$)	525	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30\text{ V}$ $V_{DS} = 30\text{ V}, T_C = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 13\text{ A}$		0.0038 0.0047	0.0044 0.0053	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	4040	-	pF
C_{OSS}	Output capacitance			740		
C_{RSS}	Reverse transfer capacitance			425		
Q_g	Total gate charge	$V_{DD} = 15\text{ V}, I_D = 26\text{ A}$ $V_{GS} = 4.5\text{ V}$ <i>Figure 19</i>	-	40	-	nC
Q_{gs}	Gate-source charge			13		nC
Q_{gd}	Gate-drain charge			16		nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	-	1.4	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=13\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ <i>Figure 13</i>		17		ns	
t_r	Rise time			18		ns	
$t_{d(off)}$	Turn-off delay time			-	75	-	ns
t_f	Fall time				46		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit	
I_{SD}	Source-drain current		-		26	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		104	A	
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=13\text{ A}$, $V_{GS}=0$	-		1.1	V	
t_{rr}	Reverse recovery time	$I_{SD}=13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ <i>Figure 15</i>		34		ns	
Q_{rr}	Reverse recovery charge			-	35		nC
I_{RRM}	Reverse recovery current				2.1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

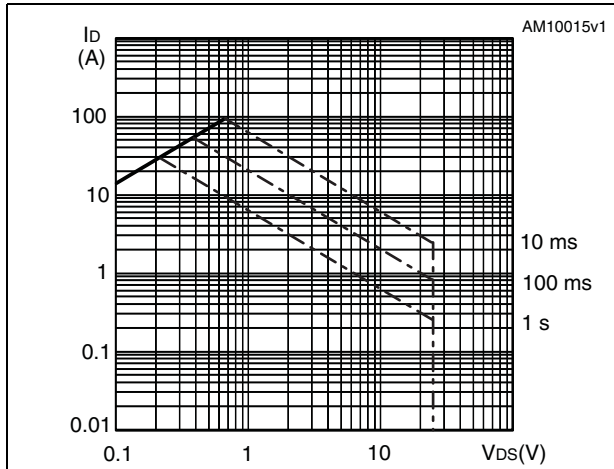


Figure 3. Thermal impedance

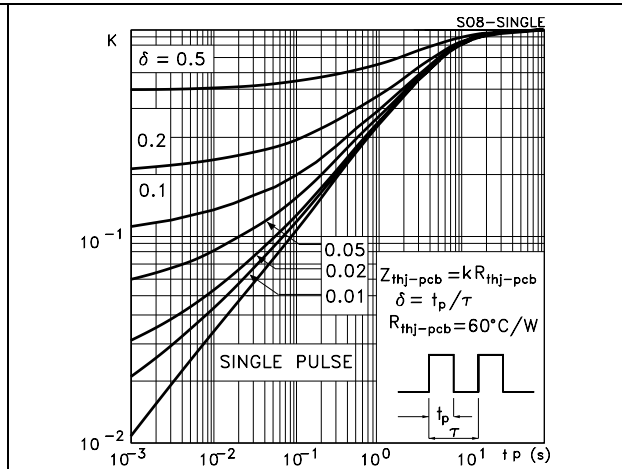


Figure 4. Output characteristics

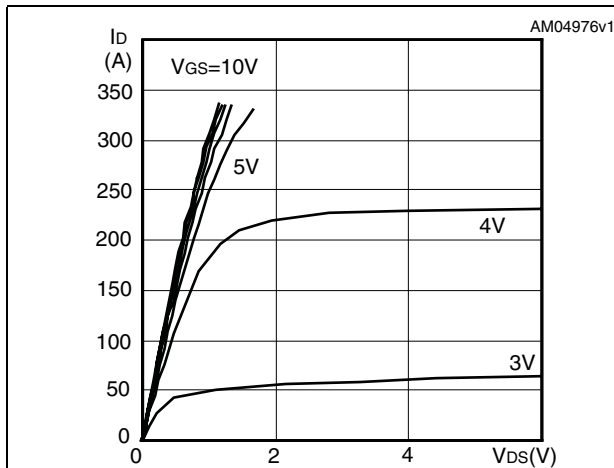


Figure 5. Transfer characteristics

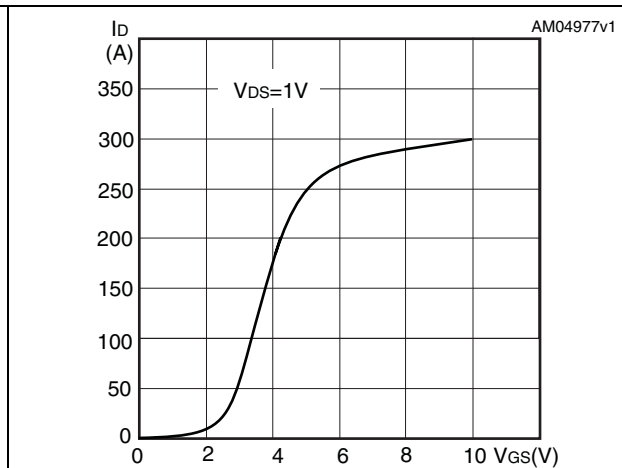


Figure 6. Normalized BV_{DSS} vs temperature

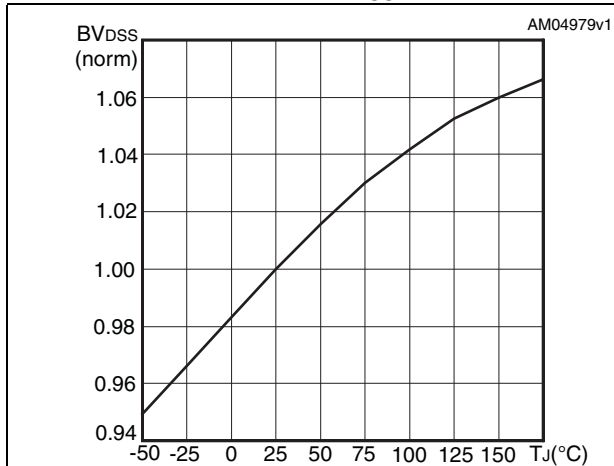


Figure 7. Static drain-source on resistance

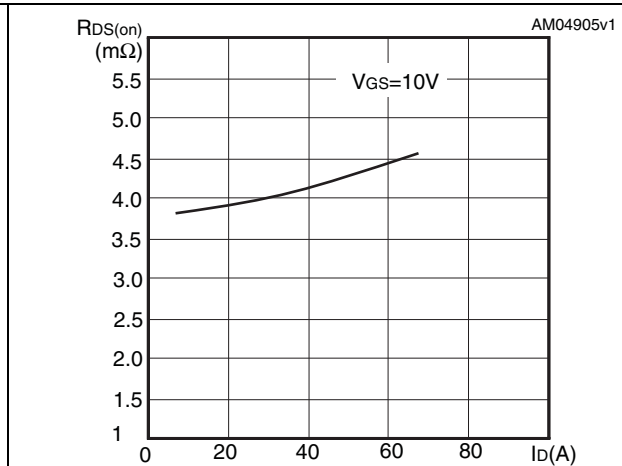


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

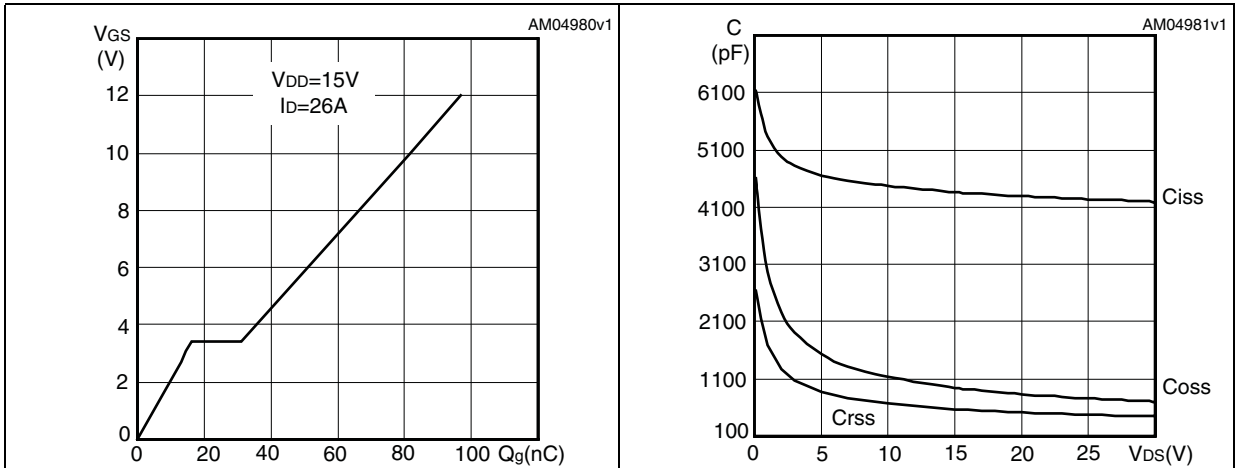


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

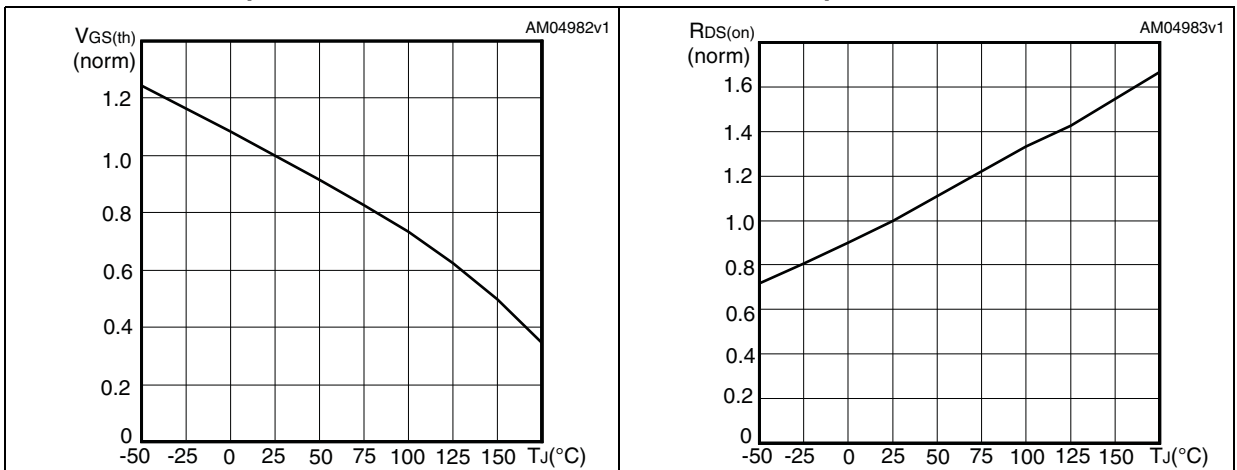
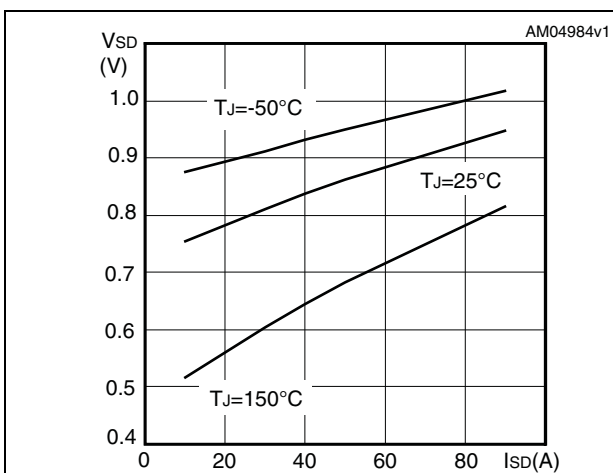


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

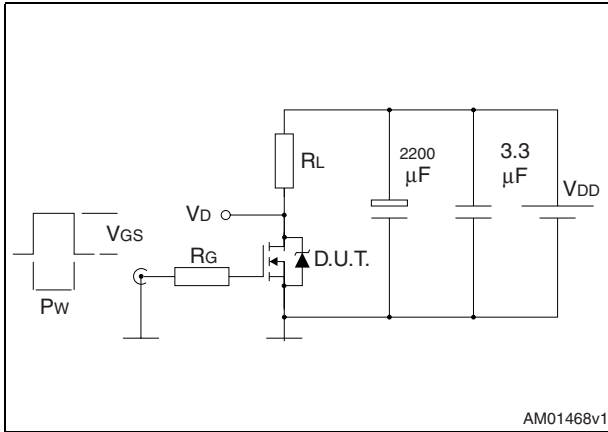


Figure 14. Gate charge test circuit

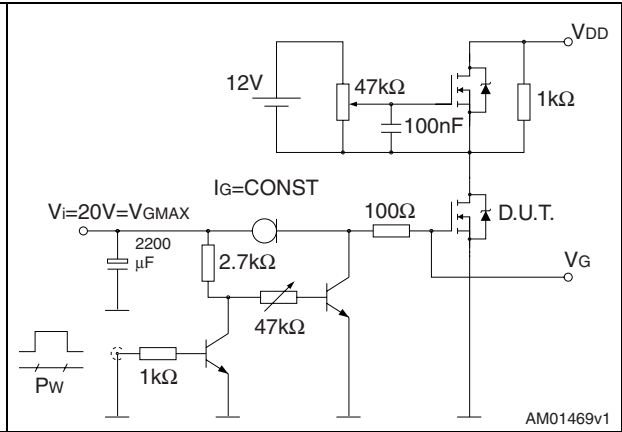


Figure 15. Test circuit for inductive load switching and diode recovery times

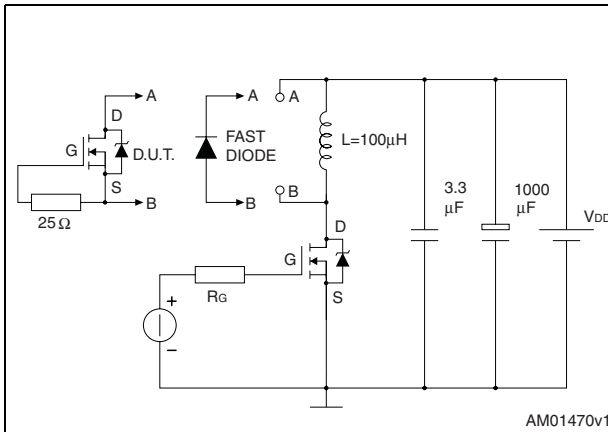


Figure 16. Unclamped inductive load test circuit

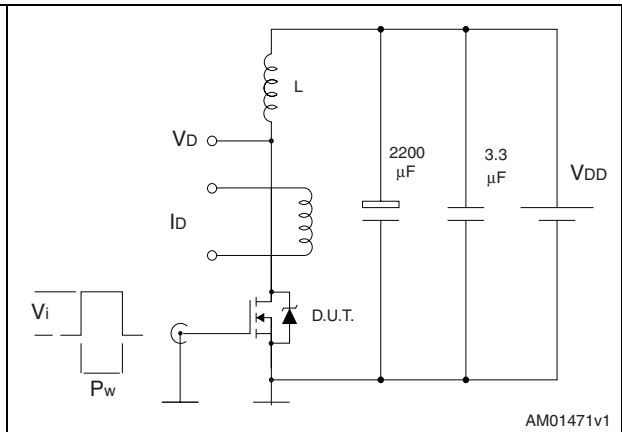


Figure 17. Unclamped inductive waveform

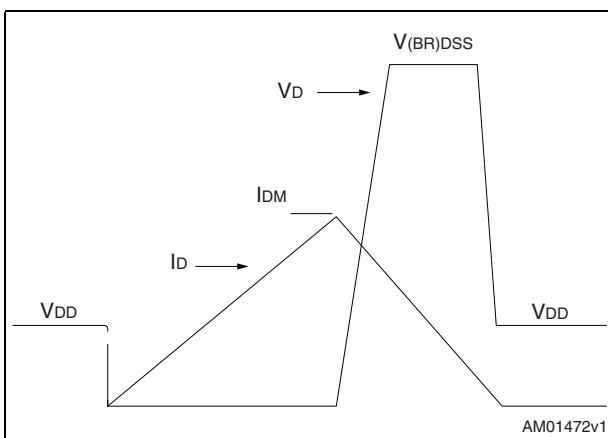


Figure 18. Switching time waveform

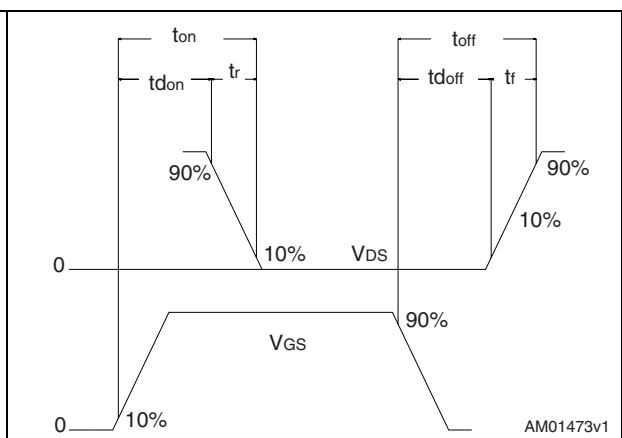
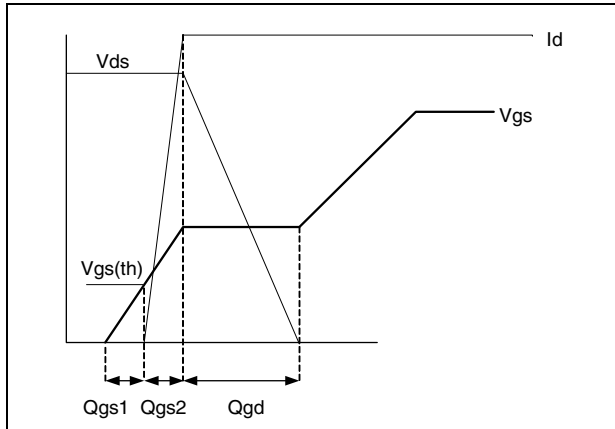


Figure 19. Gate charge waveform



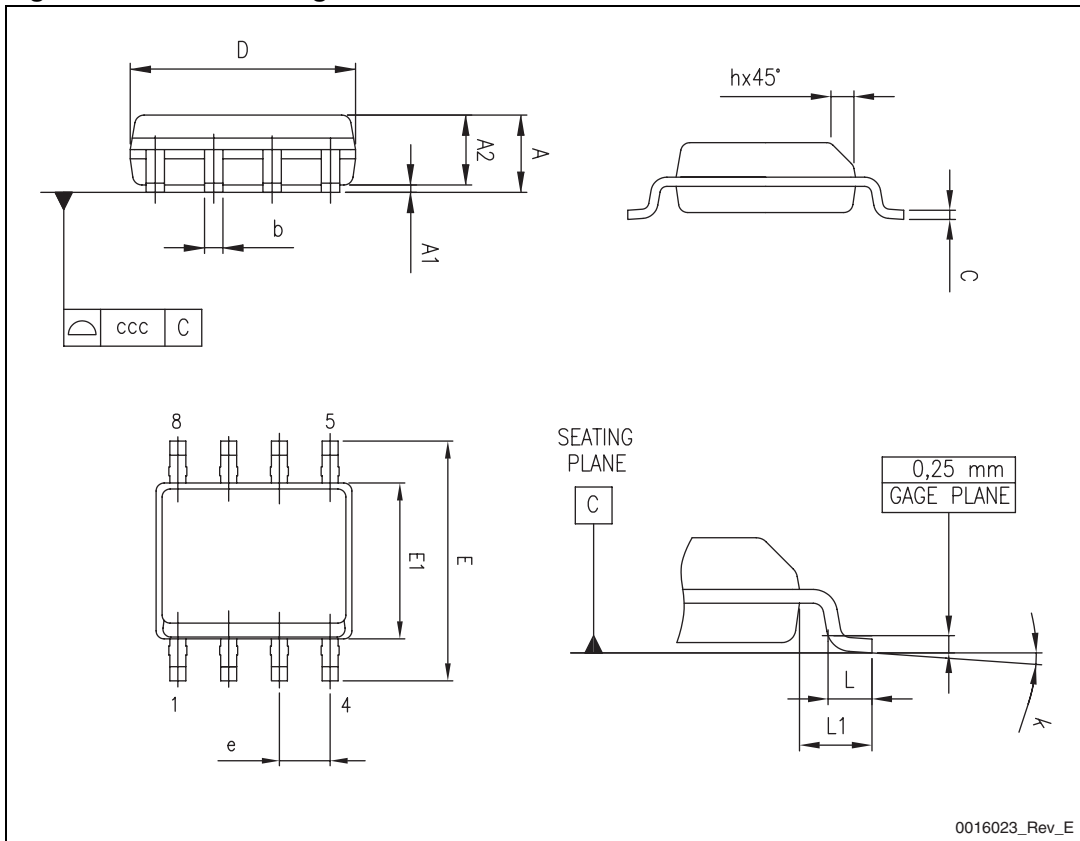
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 20. SO-8 drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-Jul-2011	1	First release.
19-Oct-2011	2	Document status promoted from preliminary data to datasheet.

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